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# User's Guide

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# Agilent Technologies E2413C MC68332 Preprocessor Interface

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# The E2413C Preprocessor Interface — At a Glance

The E2413C Preprocessor Interface provides a complete interface for state or timing analysis between any Motorola MC68332 target system and the following Agilent logic analyzers:

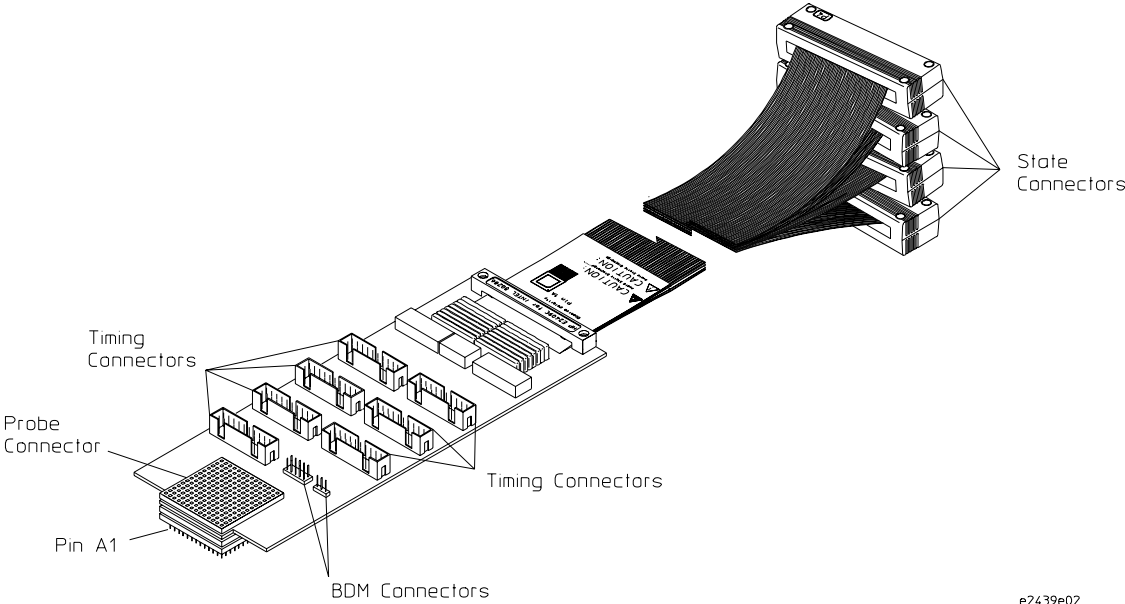
- 16540/16541A/D
- 16550A (one- or two-card)
- 16555A (one- or two-card)
- 1660A/61A/62A
- 1660AS/61AS/62AS (with oscilloscope)

For this preprocessor, two configuration files are provided for each analyzer: one for timing measurements and one for state measurements. For state measurements, an inverse assembler file converts each captured microcontroller instruction cycle into a CPU32 assembly language mnemonic.

The slide switches are used to inform the inverse assembler about the MCU configuration. The user must set these switches appropriately before making a state measurement.

The interface contains 13 connectors: 7 for timing measurements, 4 for state measurements, and 2 for background debug monitor (BDM) interface. The timing connectors present raw microcontroller signals to the logic analyzer while the state connectors present both raw and generated signals. The BDM interface provides easy connection for an external controller to view and alter microcontroller registers and system memory.

The 2413C is attached to the target system via the 132-pin QFP probe adapter or the 144-pin QFP Elastomeric probing system.



**E2413C Preprocessor Interface**

## In This Book

This book is the user's guide for the E2413C Preprocessor Interface. It assumes that you have a working knowledge of the logic analyzer used and the microcontroller being analyzed.

This user's guide is organized into three chapters:

Chapter 1 explains how to attach the preprocessor to the target and how to configure the logic analyzer for state and/or timing analysis.

Chapter 2 provides reference information on the format specification and symbols configured by the preprocessor interface software and information about the inverse assemblers and status encoding.

Chapter 3 contains reference information on the preprocessor interface hardware, including the characteristics and signal mapping for the preprocessor interface.

For more information on the logic analyzers or microcontroller, refer to the appropriate reference manual for those products.

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# Table of Contents

## **1 Setting Up the Preprocessor Interface**

Before You Begin 1-3

Setting Up the Preprocessor Interface Hardware 1-5

To power up or power down 1-6

To protect the preprocessor interface when not in use 1-6

To set the slide switches 1-7

To connect to the target system 1-9

To connect the termination adapters 1-15

To connect to the 16540/41A,D analyzer 1-16

To connect to the 16550A one-card analyzer 1-16

To connect to the 16550A two-card analyzer 1-17

To connect to the 16555A one-card analyzer 1-17

To connect to the 16555A two-card analyzer 1-18

To connect to the 1660A/AS analyzer 1-18

To connect to the 1661A/AS analyzer 1-19

To connect to the 1662A/AS analyzer 1-19

Loading the Preprocessor Interface Software 1-20

## **2 Analyzing the Motorola MC68332**

Status Bit Definition and Encodings 2-3

Using the Inverse Assembler 2-5

To synchronize the inverse assembler 2-8

Background Debug Monitor Interface 2-9

Inverse Assembler Error Messages 2-10

## **3 Preprocessor Interface Hardware Reference**

Operating Characteristics 3-3

Theory of Operation and Clocking 3-4

Signal-to-Connector Mapping 3-7

## Table of Contents

State Connector Signal Definition	3-12
Circuit Board Dimensions	3-15
Repair Strategy	3-16

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## Setting Up the Preprocessor Interface

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# Setting Up the Preprocessor Interface

This chapter explains how to set up the E2413C Preprocessor Interface hardware and software, configure the preprocessor, and connect the preprocessor to supported logic analyzers.



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## Before You Begin

This section lists the logic analyzers supported by the E2413C and provides other information about the analyzers and the preprocessor interface.

### **Equipment Supplied**

- The preprocessor interface circuit.
- The configuration and inverse assembler software on a 3.5-inch disk.
- This User's Guide.

### Minimum Equipment Required

- The E2413C preprocessor interface and inverse assembler.
- The 132-pin QFP probe adapter or the 144-pin QFP Elastomeric Probing System.
- The configuration and inverse assembler software on a 3.5-inch disk.
- One of the logic analyzers listed in the following table:

**Table 1-1 Logic Analyzers Supported**

Logic Analyzer	Channel Count	State Speed	Timing Speed	Memory Depth
<b>16540/41A,D</b>	112	100 MHz	100 MHz	4 k states (A version) 16 k states (D version)
<b>16550A (one card)</b>	102	100 MHz	250 MHz	4 k states
<b>16550A (two card)</b>	204	100 MHz	250 MHz	4 k states
<b>16555A (one card)</b>	68	100 MHz	250 MHz	1 M states
<b>16555A (two card)</b>	136	100 MHz	250 MHz	1 M states
<b>1660A/AS</b>	136	100 MHz	250 MHz	4 k states
<b>1661A/AS</b>	102	100 MHz	250 MHz	4 k states
<b>1662A/AS</b>	68	100 MHz	250 MHz	4 k states

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## Setting Up the Preprocessor Interface Hardware

Setting up the preprocessor interface hardware consists of the following major steps:

- Turn off the logic analyzer and the target system.

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**CAUTION**

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To protect your equipment, remove the power from both the logic analyzer and the target system before you make or break connections. Because the logic analyzer supplies power to the preprocessor interface, the logic analyzer should always be powered up before the target system; when powering down, power down the target system first and then power down the logic analyzer.

- Set the slide switches on the top of the preprocessor interface according to the configuration of the MC68332.
- Attach the probe to the target system.
- Attach the preprocessor interface to the probe.
- Connect the logic analyzer pods to the cable connectors of the preprocessor interface board.
- Load the appropriate configuration file.

Please see Table 1-2 on page 1-24 for corresponding files.

The remainder of this section describes these general steps in more detail.

## To power up or power down

When powering up, the logic analyzer must be powered up first, followed by the target system. The logic analyzer provides the power to the active circuits on the preprocessor interface. Unpowered circuits may cause improper operation of the target system.

When powering down, the target system should be powered down first, followed by the logic analyzer.

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## To protect the preprocessor interface when not in use

- **Cover the socket assembly pins of the preprocessor interface with a conductive foam wafer or conductive plastic pin protector.**

The socket assembly pins of the preprocessor interface were covered at the time of shipment with either a conductive foam wafer or conductive pin protector. If this device is not damaged, it may be reused repeatedly.

- **Store the preprocessor interface in an antistatic bag or container.**

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### **CAUTION**

**Electrostatic Discharge.** The socket assembly pins of the preprocessor interface should be covered with a conductive foam wafer or pin protector to protect the delicate gold plated pins of the assembly from damage due to impact. Covering the pins and properly storing the preprocessor interface also protects the active circuitry on the preprocessor interface from electrostatic discharge.

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## To set the slide switches

The slide switches are used to inform the inverse assembler about the MCU configuration when making state measurements. The switches perform three functions. First, they validate a multi-function pin as an MCU signal versus a general purpose input/output for direct use by the inverse assembler. Second, they validate a multi-function pin as an MCU signal versus a general purpose input/output for use in generating signals to be used by the inverse assembler. Third, the slide switches direct the logic analyzer to capture bus cycles generated by other bus masters and/or debug controllers. They must be set appropriately or the output of the inverse assembler cannot be guaranteed.

The overlay supplied with the preprocessor card labels the function of each switch and shows the position of valid and invalid settings. You may wish to refer to it as each switch is being discussed below.

- **If the MC68332 configuration is using any of the chip selects, set the associated switch to the VALID position. Set all others to the INVALID position.**

Eleven switches validate the chip select signals (CS0-10).

Six switches are used to validate control signals from the MCU. They are: SIZ0, SIZ1, DSACK0, DSACK1, AS, and DS.

Two switches are used to capture bus cycles not associated with the execution of user code. ACQNONMCU controls whether the logic analyzer acquires bus cycles caused by other bus masters in the target system (BGACK asserted). ACQBKGND controls whether the logic analyzer acquires bus cycles caused by a controller performing debug commands (FREEZE asserted).

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**Note:**

Signals A19—A23 and CS6—CS10 are multiplexed onto the same pins, and the default configuration of the logic analyzer assumes that signals A19—A23 are valid. If any of the chip selects, CS6—CS10, are being used and the appropriate switch(es) are set to VALID on the preprocessor, then the bits associated with A19—A23 should be removed from the ADDR label via the format menu in the logic analyzer. This corresponds to bits 3—7 of pod A4. This results in the display of correct address information in the ADDR field of the listing menu and presents only valid address bus bits to the ADDR field in the trigger menu.

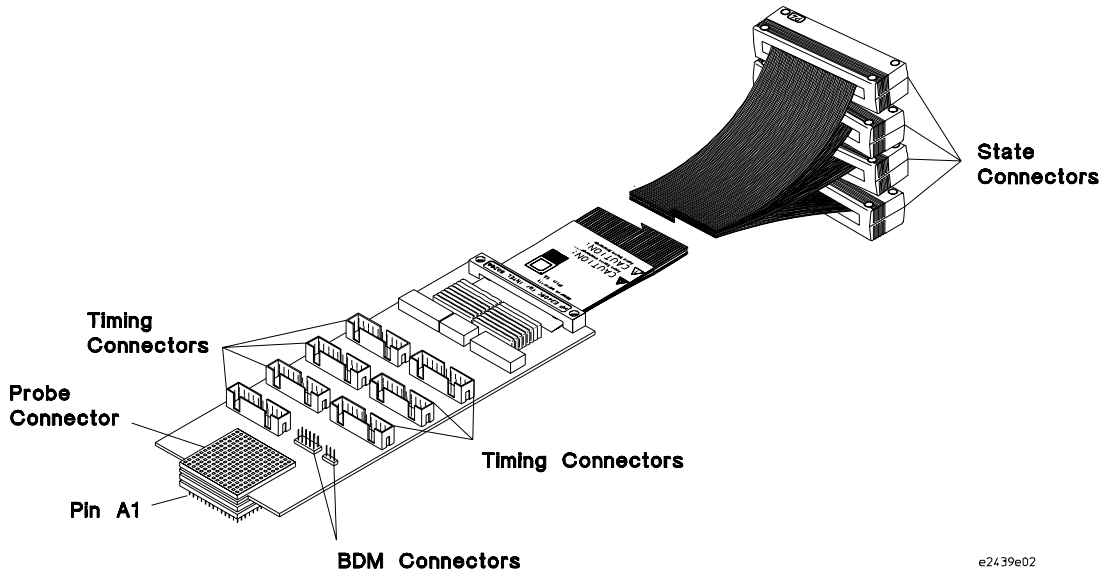
Setting Up the Preprocessor Interface  
To set the slide switches

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**Note:** In order to distinguish between internal and external bus cycles, the preprocessor must have one of the following combinations: DS and AS must be valid or DS and at least one CS must be valid. If DS is the only valid control signal, all cycles will be interpreted as internal cycles.

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- If the MC68332 configuration is using BGACK and/or FREEZE, set the associated switch to the VALID position. Otherwise, set the associated switch to the INVALID position.



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**E2413C Preprocessor Interface Assembly**

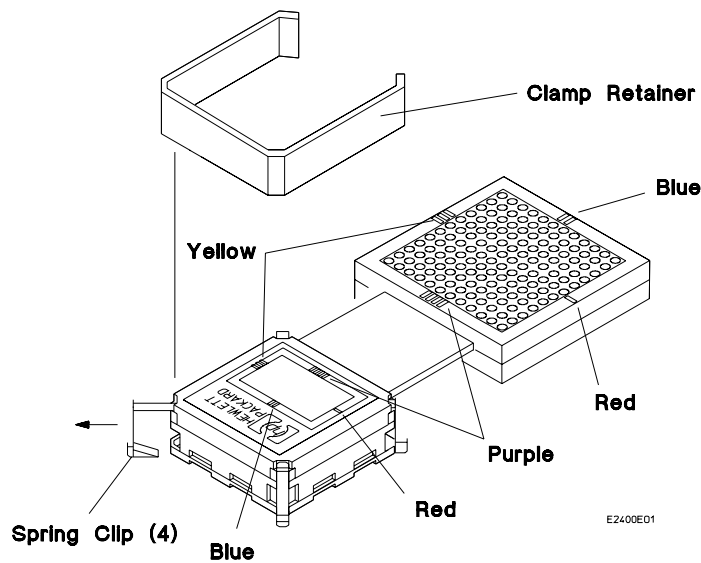
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## To connect to the target system

The preprocessor interface requires a probe adapter for connecting to the MC68332 microcontroller. The E2413C MC68332 preprocessor supports connecting to a 132-pin PQFP using a QFP Probe Adapter Assembly. It also supports connecting to a 144-pin TQFP using the E5336A QFP Elastomeric Probing System.

### Connecting using a QFP Probe Adapter Assembly

The 132-pin QFP probe adapter assembly allows the preprocessor interface to be connected without removing the microcontroller from the target system.



### 132-Pin QFP Probe Adapter Assembly

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**CAUTION**

Serious damage to the target system or preprocessor interface can result from incorrect connection. Note the position of pin 1 on the microcontroller and pin A1 on the preprocessor interface prior to making any connection. Ensure proper connection by making sure the pins are aligned and seated correctly in sockets.

**To connect to the target system**

- Prevent equipment damage by removing power from both the logic analyzer and the target system.
- Use the instructions in the *QFP Probe Adapter Assembly* manual to connect the 132-pin QFP probe adapter assembly to the target system microcontroller.
- Install the preprocessor interface into the PGA socket on the probe adapter.

**To rotate the 132-pin PQFP probe adapter**

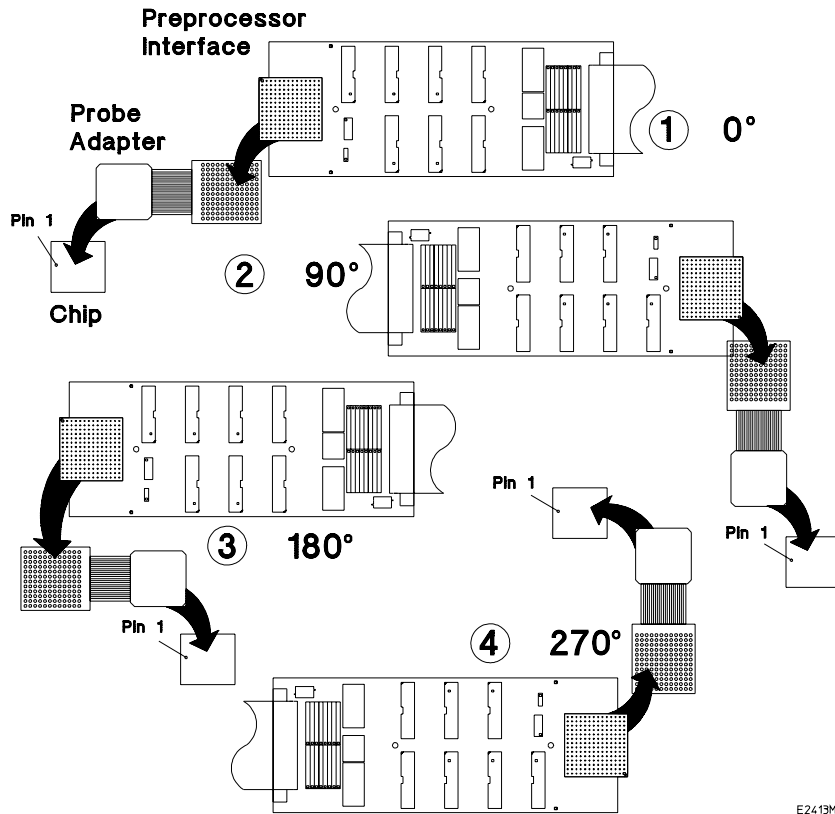
- Connect the adapter and preprocessor in one of the rotations shown below.

The E2413C supports rotations of 0, 90, 180, and 270 degrees.

- Rotate the adapter, with respect to the microcontroller, the desired number of degrees.
- Rotate the preprocessor, with respect to the adapter, the same number of degrees.

Rotation and, perhaps, the use of additional PGA pin protector adapters can allow you to clamp onto a difficult to reach part.





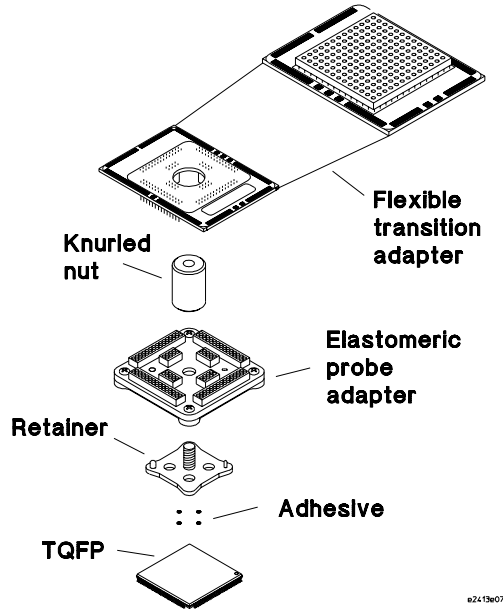
E2413M10

132-Pin PQFP Probe Adapter Rotation Diagram

Setting Up the Preprocessor Interface  
**To connect to the target system**

**Connecting using the E5336A QFP Elastomeric Probing System**

The 144-pin QFP Elastomeric Probing System allows the preprocessor interface to be connected without removing the microcontroller from the target system.



**144-Pin QFP Probing System**

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**CAUTION**

Serious damage to the target system or preprocessor interface can result from incorrect connection. Note the position of pin 1 on the microcontroller and pin A1 on the preprocessor interface prior to making any connection. Ensure proper connection by making sure the pins are aligned and seated correctly in sockets.

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**CAUTION**

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- Prevent equipment damage by removing power from both the logic analyzer and the target system.

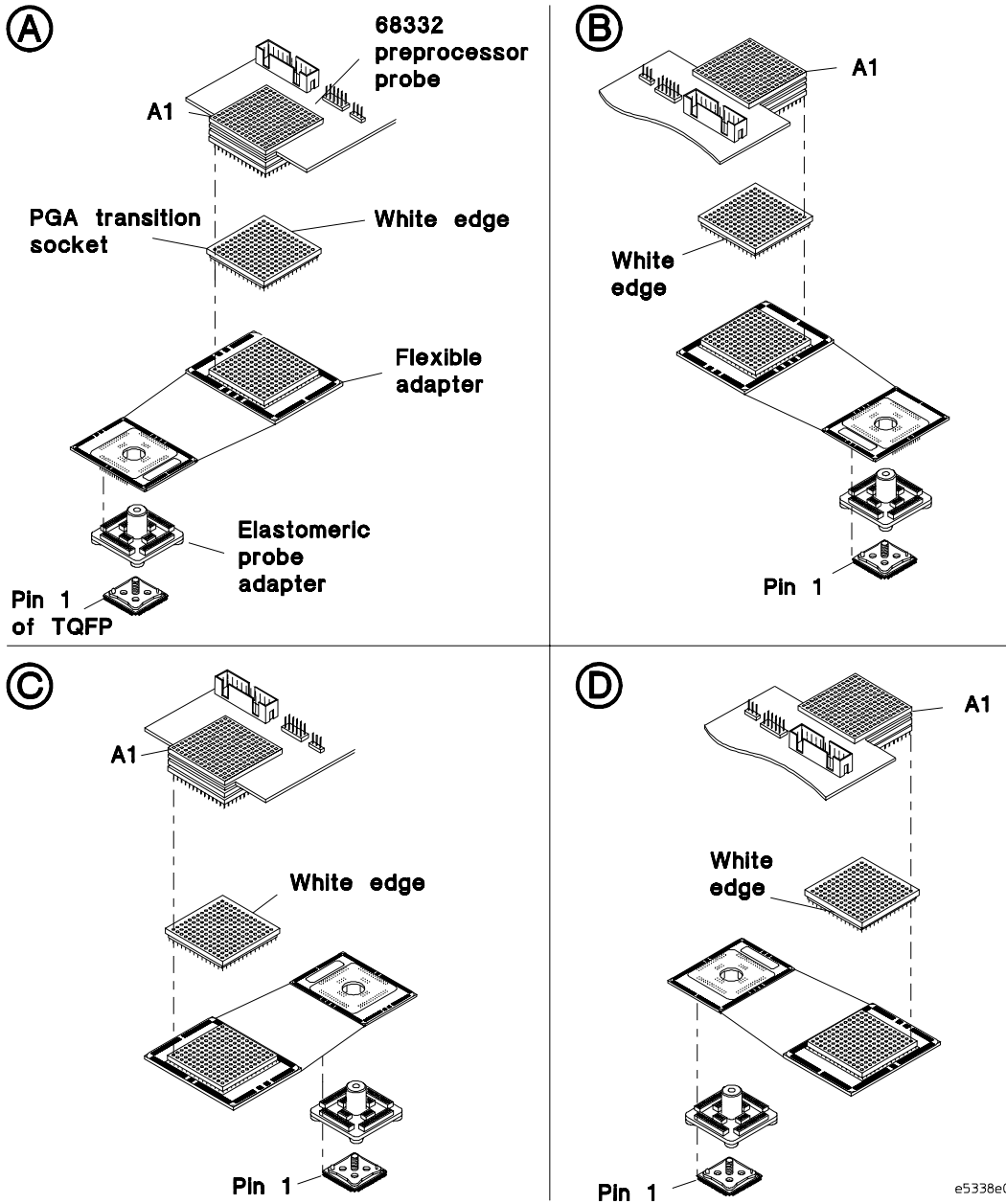
Serious damage to the target system or preprocessor interface can result from incorrect connection.

- Follow the instructions in the *QFP Elastomeric Probing System* manual to install the probe adapter onto your QFP. The major steps are:
  - Prepare to attach the retainer to the QFP.
  - Test the alignment before adhering the retainer.
  - Adhere the retainer to the QFP.
  - Install the probe adapter
- Refer to the illustration on the following page to select the orientation which allows the best access to your TQFP.

**Disregard color/bar coding.** Follow the illustration on the following page. The color/bar coding does not apply in this instance.

- Attach the flexible transition adapter to the probe adapter maintaining the selected orientation.
- Install the preprocessor interface into the PGA socket on the flexible transition adapter.

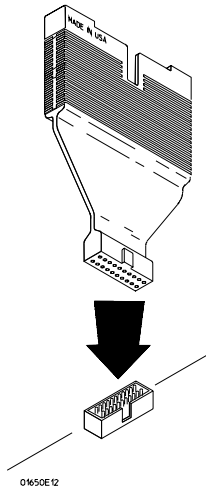
Setting Up the Preprocessor Interface  
To connect to the target system



144-Pin TQFP Probing System Rotation Diagram

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## To connect the termination adapters



### Connecting the Termination Adapter

- Align the key on the male end of the termination adapter with the slot on the connector of one of the logic analyzer cables. Push the termination adapter into the connector.
- Connect the female end of the termination adapter to the preprocessor interface.

The logic analyzer probes must be terminated for correct operation.

The nonterminated connectors, P1 through P7, must be probed by using either the General Purpose probes (shipped with the logic analyzer) or the 100 kOhm Termination Adapters (part number 01650-63203).

Setting Up the Preprocessor Interface  
**To connect to the 16540/41A,D analyzer**

**To connect to the 16540/41A,D analyzer**

**1. Connect the pod cables to the preprocessor interface according to the pod diagram below.**

16540/41A,D Logic Analyzer	E2413B Preprocessor	Mode
Pod4	P1	STATE
Pod3	P2	STATE
Pod4	P3	STATE
Pod2	P4	TIMING
Master Pod1	P1	TIMING
Expansion1 Pod1-3	P2-4	TIMING
Expansion2 Pod1-3	P5-7	TIMING

**2. For **state**, load configuration file E68332S. For **timing**, load configuration file E68332T.**

**To connect to the 16550A one-card analyzer**

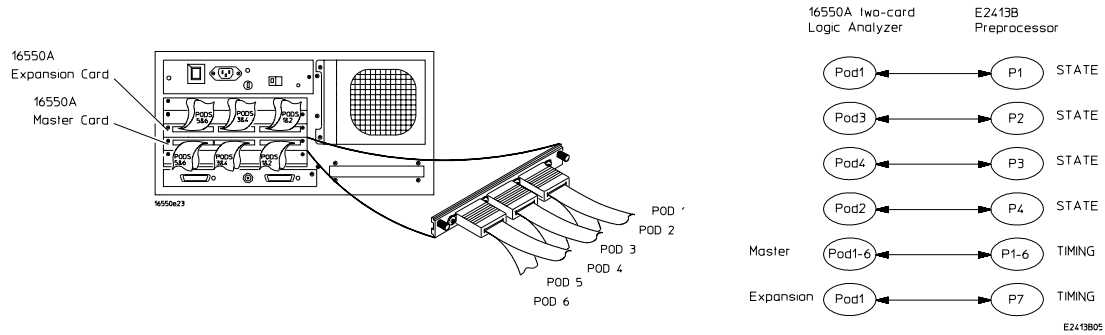
**1. Connect the pod cables to the preprocessor interface according to the pod diagram below.**

16550A one-card Logic Analyzer	E2413B Preprocessor	Mode
Pod1	P1	STATE
Pod3	P2	STATE
Pod4	P3	STATE
Pod2	P4	STATE
Pod1-6	P1-6	TIMING

**2. For **state**, load configuration file F68332S. For **timing**, load configuration file F68332T.**

## To connect to the 16550A two-card analyzer

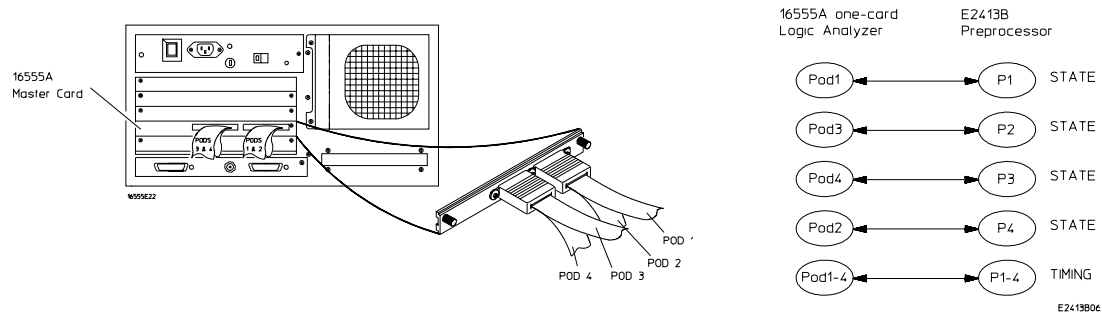
1. Connect the pod cables to the preprocessor interface according to the pod diagram below.



2. For **state**, load configuration file F68332S. For **timing**, load configuration file F68332T.

## To connect to the 16555A one-card analyzer

1. Connect the pod cables to the preprocessor interface according to the pod diagram below.



2. For **state**, load configuration file M68332S. For **timing**, load configuration file M68332T.

Setting Up the Preprocessor Interface  
**To connect to the 16555A two-card analyzer**

**To connect to the 16555A two-card analyzer**

**1. Connect the pod cables to the preprocessor interface according to the pod diagram below.**

**2. For *state*, load configuration file M68332S. For *timing*, load configuration file M68332T.**

**To connect to the 1660A/AS analyzer**

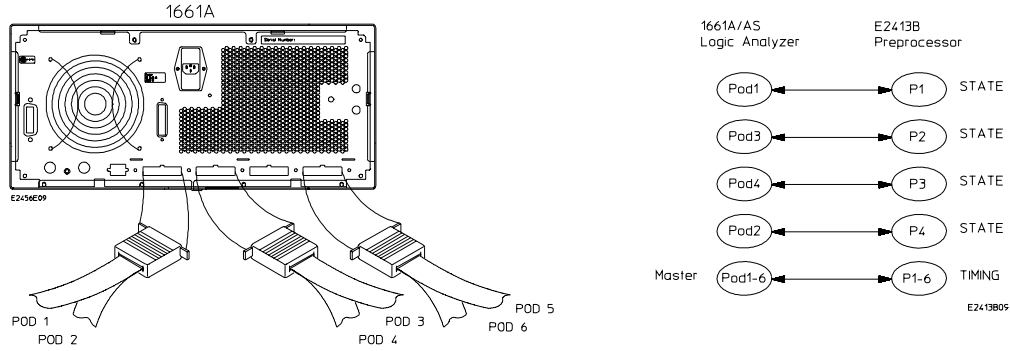
**1. Connect the pod cables to the preprocessor interface according to the pod diagram below.**

**2. For *state*, load configuration file F68332S. For *timing*, load configuration file F68332T.**



## To connect to the 1661A/AS analyzer

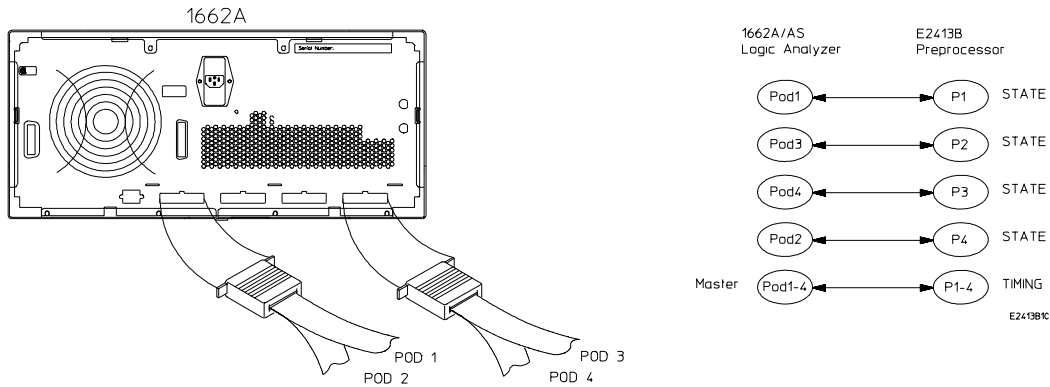
1. Connect the pod cables to the preprocessor interface according to the pod diagram below.



2. For **state**, load configuration file F68332S. For **timing**, load configuration file F68332T.

## To connect to the 1662A/AS analyzer

1. Connect the pod cables to the preprocessor interface according to the pod diagram below.



2. For **state**, load configuration file F68332S. For **timing**, load configuration file F68332T.

## Loading the Preprocessor Interface Software

Loading the preprocessor interface software consists of the following steps:

- **Make a duplicate copy of the master disk prior to setting up the preprocessor interface.**
- **Insert the preprocessor interface disk in the disk drive of the logic analyzer.**
- **Select the appropriate menu for loading files for state and timing analysis.**
- **Use the knob to select the appropriate configuration file.**

Choosing the correct configuration file depends on which analyzer you are using and whether or not you need timing and/or state analysis. The software version(s) of your analyzer software also affects your configuration file choice. See the applicable subsection in the previous section.

- **Execute the load operation to load the file into the logic analyzer.**

The logic analyzer is configured for MC68332 analysis by loading the appropriate MC68332 configuration file. Loading this file also automatically loads the inverse assembler for state configurations.

The table on the following page lists the correct configuration file to for each logic analyzer.

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**Table 1-2 Logic Analyzer Configuration Files**

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<b>Logic Analyzer</b>	<b>Timing Configuration File</b>	<b>State Configuration File</b>
<b>16540/41A,D</b>	E68332T	E68332S
<b>16550A (one card)</b>	F68332T	F68332S
<b>16550A (two card)</b>	F68332T	F68332S
<b>16555A (one card)</b>	M68332T	M68332S
<b>16555A (two card)</b>	M68332T	M68332S
<b>1660A/AS</b>	F68332T	F68332S
<b>1661A/AS</b>	F68332T	F68332S
<b>1662A/AS</b>	F68332T	F68332S



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Analyzing the Motorola  
MC68332

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# Analyzing the Motorola MC68332

This chapter describes preprocessor interface data, symbol encodings, and information about the available inverse assemblers.

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## Status Bit Definition and Encodings

This section describes symbol information that has been set up by the preprocessor interface configuration software and information about the available inverse assemblers including filtering and debug monitors.

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**Table 2-1 MC68332 Status Bit Description**

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<b>Bit</b>	<b>Status Symbol</b>	<b>Description</b>
<b>0</b>	~SHOW_CYCLE	Indicates an internal MCU cycle.
<b>1</b>	Rd/~Wr	Indicates the direction of data transfer.
<b>2</b>	~INST_FETCH	Indicates an instruction fetch.
<b>3</b>	~PIPE_FLUSH	Indicates an instruction caused an instruction pipeline flush.
<b>4, 5</b>	SIZE0/1	Indicates the number of bytes in a transfer.
<b>6</b>	~SIZE0_VALID	Indicates that the MCU is configured to supply SIZE0.
<b>7</b>	~SIZE1_VALID	Indicates that the MCU is configured to supply SIZE1.
<b>8, 9</b>	~DSACK0/1	Indicates the number of bytes accepted/provided in a transfer.
<b>10</b>	~BErr	Indicates a bus error for a particular cycle.
<b>11</b>	~BUS_CONTROL_INVALID	Indicates that the MCU is not configured to supply ~BR, ~BG, and ~BGACK.
<b>12</b>	~FCx_INVALID	Indicates that the MCU is not configured to supply FC0, FC1, and FC2.
<b>13</b>	~A19_THRU_A23_INVALID	Indicates that the MCU is not configured to supply A19-A23.
<b>14</b>	FREEZE	When asserted, indicates the MCU is operating in background mode. When negated, indicates normal mode.
<b>15</b>	~BKPT	When asserted, indicates the MCU has encountered a hardware breakpoint.

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**Table 2-2 MC68332 Symbolic Representation of Status Bits**

Label	Symbol	Status Encoding
<b>Cycle Type</b>	Opcode Fetch (internal)	x x x 2 H or x x x A H
	(external)	x x x 3 H or x x x B H
	Data Read (internal)	x x x 6 H or x x x E H
	(external)	x x x 7 H or x x x F H
	Data Write (internal)	x x x 4 H or x x x C H
	(external)	x x x 5 H or x x x D H
<b>Size of Transfer</b>	Byte Transfer (8 bit)	x x 1 x H
	Word Transfer (16 bit)	x x 2 x H
	3-Byte Transfer (24 bit)	x x 3 x H
	Long Word Transfer (32 bit)	x x 0 x H

**Note:**

The logic analyzer captures prefetches even if they are not executed. Care must be taken when specifying a trigger condition or a storage qualification that follows an instruction that may cause branching. An unused prefetch may generate an unwanted trigger.

Since the microcontroller only prefetches at most two words, one technique to avoid unwanted triggering from unused prefetches is to add "4" to the trigger address. This trigger condition will only be satisfied if the branch is not taken.



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# Using the Inverse Assembler

This section discusses the general output format of the inverse assembler and controller-specific information. This section also assumes that an inverse assembly has been loaded.

The MC68332 microcontroller does not indicate externally which word fetched is the beginning of a new instruction. You may have to "point" to the first state of an instruction fetch to synchronize the inverse assembler. Once synchronized, the inverse assembler will disassemble from this state through the end of the screen. See "To synchronize the inverse assembler" on page 2-8 for more information.

## **General Output Format**

The next few paragraphs describe the general output format of the inverse assemblers.

### **Numeric Format**

Unless a value is followed by a suffix character, numeric output from the inverse assembler is in hexadecimal format. For example, decimal values have a period (.) as the suffix character; binary values have a percent sign (%).

### **Missing Opcodes/Operands**

Asterisks (\*) in the inverse assembler output indicate missing operands. Missing operands occur frequently and are primarily due to microcontroller prefetch activity. Storage qualification or the use of storage windows can also lead to such occurrences.

**Don't Care Bytes**

The MC68332 microcontroller can perform 3-byte transfers. During operand reads and writes, entire 16-bit (word) values appear on the microcontroller data bus lines. The inverse assembler will attempt to display "xx" for any bytes in a transfer that are ignored by the microcontroller. You can then determine exactly which byte or bytes of data were used as an operand. If the microcontroller is configured such that the number of bytes being transferred cannot be determined, an entire word will be displayed. You must then determine which bytes are valid.

**Unexecuted Prefetched Instructions**

Prefetched instructions which are not executed by the microcontroller are marked by a hyphen "-" in the first column of the mnemonic/hex field

**Processor-Specific Output Format**

This section discusses issues specific to the MC68332 inverse assembler.

Acquisitions of coprocessor and background cycles may be individually enabled/disabled.

A "c" marks coprocessor activity and background activity is marked with a "b". The "c" and "b" are displayed in the first column of the mnemonic/hex field.

**General Missing Terms**

Depending on the configuration of the microcontroller, the inverse assembler may be unable to supply all the of the information it can supply. For example, if ~DS (data strobe) is not valid, internal cycles cannot be captured.

Additionally, if the function control pins FC0, 1, and 2 are configured as chip selects, question marks will be substituted for "user" and "supr" terms.

### **Filtering**

The MC68332 inverse assembler is capable of suppressing certain acquired buses and cycles from the display thus allowing the user to focus on and display more cycles of interest. The filter softkeys are part of the "Invasm Options" submenu. "Invasm Options" must be pressed to display the submenu.

Cycle suppression is broken down into the following categories: extension words, unexecuted prefetches, branches, calls and returns, other instructions, data reads, and data writes.

Extension words and unexecuted fetches are suppressed without regard to user mode or supervisor mode because they do not affect the display of executed mnemonics.

All other categories may suppress based on the user mode, supervisor mode, or both. These categories suppress actual executed mnemonics for the display.

### **Controller Configurations**

The E2413C preprocessor interface and inverse assembler will support any MC68332 configuration except those that use a Port C signal as a general purpose input/output.

## To synchronize the inverse assembler

- Identify a line on the display that you know is the first state of an instruction fetch.
- Roll this line to the top of the listing.
- Press the Invasm field at the top of the screen.

This will cause the Invasm Options submenu to appear.

- Press the Align softkey.

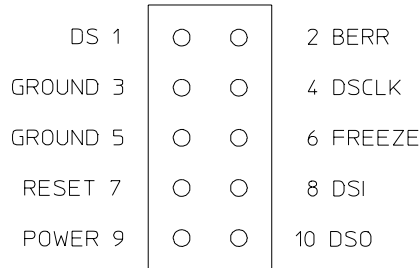
The listing will inverse assemble from the top line down. Any data before this screen is left unchanged. Rolling the screen up will inverse assemble the lines as they appear on the bottom of the screen. If you jump to another area of the listing by entering a new line number or by rolling the screen down, you may have to re-synchronize the inverse assembler by repeating the described steps.

Each time you inverse assemble a block of memory, the analyzer will keep that block in the inverse assembled condition. You can inverse assemble several different blocks in the analyzer memory, but the activity between those blocks will not be inverse assembled.

---

## Background Debug Monitor Interface

The background debug monitor (BDM) interface allows an external controller to connect to and control the microcontroller through the preprocessor. The 10-pin BDM connector is defined in the following figure.



E2413B11

### Background Debug Monitor Interface Diagram

External to the preprocessor, the BDM needs to be supplied with voltage (either 5V or 3.3V) from the preprocessor. The 3-pin connector (J2) allows the user to select the supply voltage sent to the BDM interface. If the 2-pin jumper is connected between pins 1 and 2, 5V is connected. If the jumper is connected between pins 2 and 3, the voltage of the MC68332 is connected. It is assumed that if the BDM hardware is operating at 3.3V, the MC68332 is also a 3.3V device. If, however, the MC68332 is a 5V device and the BDM hardware is 3.3V, the jumper may be removed and a 3.3V source may be attached to pin 2 of J2.

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# Inverse Assembler Error Messages

Any of the following list of error messages may appear during analysis of your target software. Included with each message is a brief explanation.

## **Fatal Data Error**

Displayed if the trace memory could not be read properly on entry into the inverse assembler.

## **Illegal Opcode <code>**

Displayed if the inverse assembler encounters an illegal instruction.

## **Reserved Opcode**

Displayed if the inverse assembler encounters a reserved coprocessor instruction.

## **Incomplete Opcode**

Displayed if the inverse assembly cannot acquire all words of a multi-word instruction.

## **\*s**

Displayed if the inverse assembler cannot find a complete operand field for an instruction. Prefetch activity or storage qualification is often the cause.

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Preprocessor Interface  
Hardware Reference

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# Preprocessor Interface

## Hardware Reference

This chapter contains reference information on the 2413C hardware including product, electrical, and environmental characteristics, signal mapping, a brief theory of operation, circuit board dimensions, and repair information.



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## Operating Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the preprocessor interface.

### Product Characteristics

Microcontroller Supported	Motorola MC68332
Package Supported	132-pin PQFP 144-pin TQFP
Probes Required	Mandatory 4 for state. Up to 7 for timing.
Accessories Required	5081-7736 Probe Adapter for 132-pin PQFP. QFP Elastomeric Probing System for 144-pin TQFP (see replaceable parts list for part numbers). One 01650-63203 Termination Adapter for each pod used for timing measurements.

### Electrical Characteristics

Power Requirements	250mA typical @ 5V, supplied by logic analyzer.
Signal Line Loading	8pF maximum on all signals except CLKOUT which has 40pF maximum.

### Environmental Characteristics

Temperature	Operating	0 to + 55 degrees C +32 to +131 degrees F
	Nonoperating	-40 to + 75 degrees C -40 to +167 degrees F
Altitude	Operating	4,600 m 15,000 feet
	Nonoperating	15,3000 m 50,000 feet
Humidity	Up to 90% noncondensing. Avoid sudden , extreme temperature changes which could cause condensation on the circuit board.	

## Theory of Operation and Clocking

For timing measurements, raw digital signals from the MC68332 are presented to the logic analyzer through the timing connectors. The acquisition clock is provided by the logic analyzer.

For state measurements, raw digital signals from the MC68332 and generated signals from the programmable logic are latched and presented to the logic analyzer through the state connectors. The acquisition clock is generated by the programmable logic.

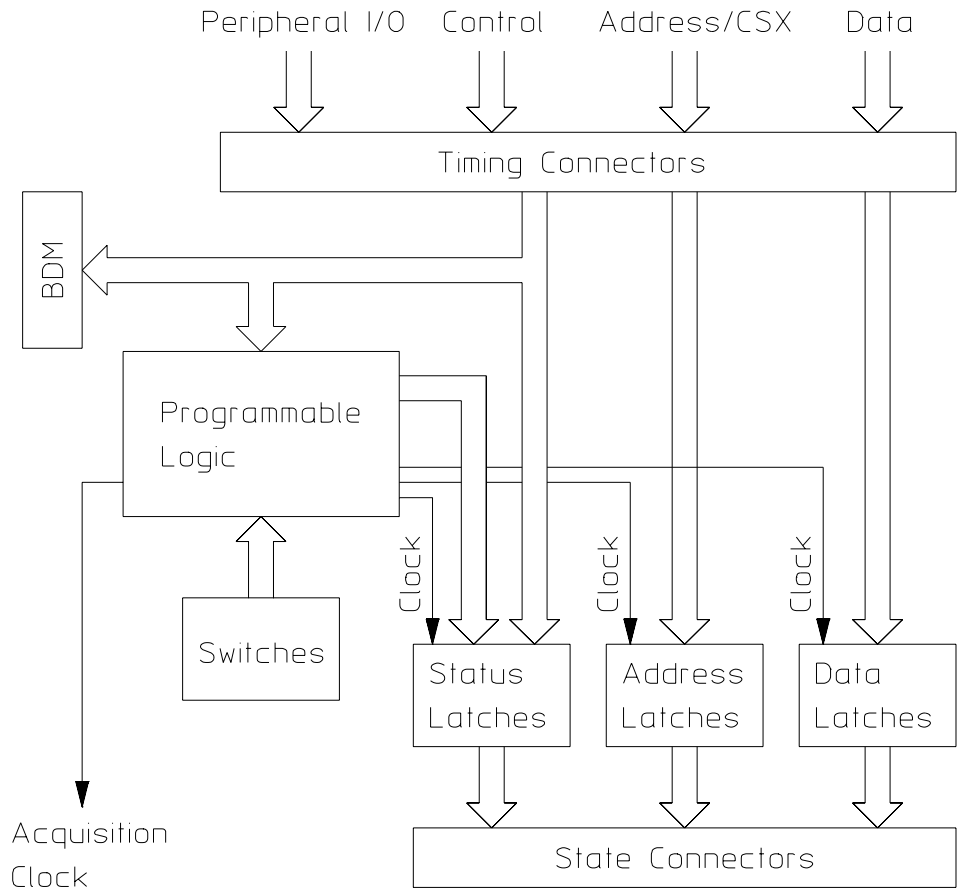
As can be seen in the timing diagram on page 3-6, all state information (data, address, and status) for external cycles (normal and fast termination) is available within the bus cycle. For internal cycles (also known as show cycles), however, data is not available until after the completion of the bus cycle. To capture both internal and external cycles with a single acquisition clock, all timing must conform to the internal cycle case. The acquisition clock must be delayed until a clock after any bus cycle completes. In turn, all state information must be latched.

Signals that could be used in address calculations, including address, chip selects, and function codes, are latched at the same time. Although bus control signals could be active and latched with this group, BGACK is the only signal of importance and, if asserted, prevents the microcontroller from controlling the bus.

Status signals are latched at the end of the bus cycle and at the same time to minimize logic. While most status signals are valid much sooner, BERR and BKPT are valid only at the end.

Data must be latched separately because it becomes valid at two different times.

The acquisition clock is always generated one clock after the end of a bus cycle. For address and status, and data on external cycles, this simply means extra set-up time. For internal cycles, it means that data is aligned with its associated address and status. Any combination of state signals may be specified in the trigger menu to find either an internal or external cycle.



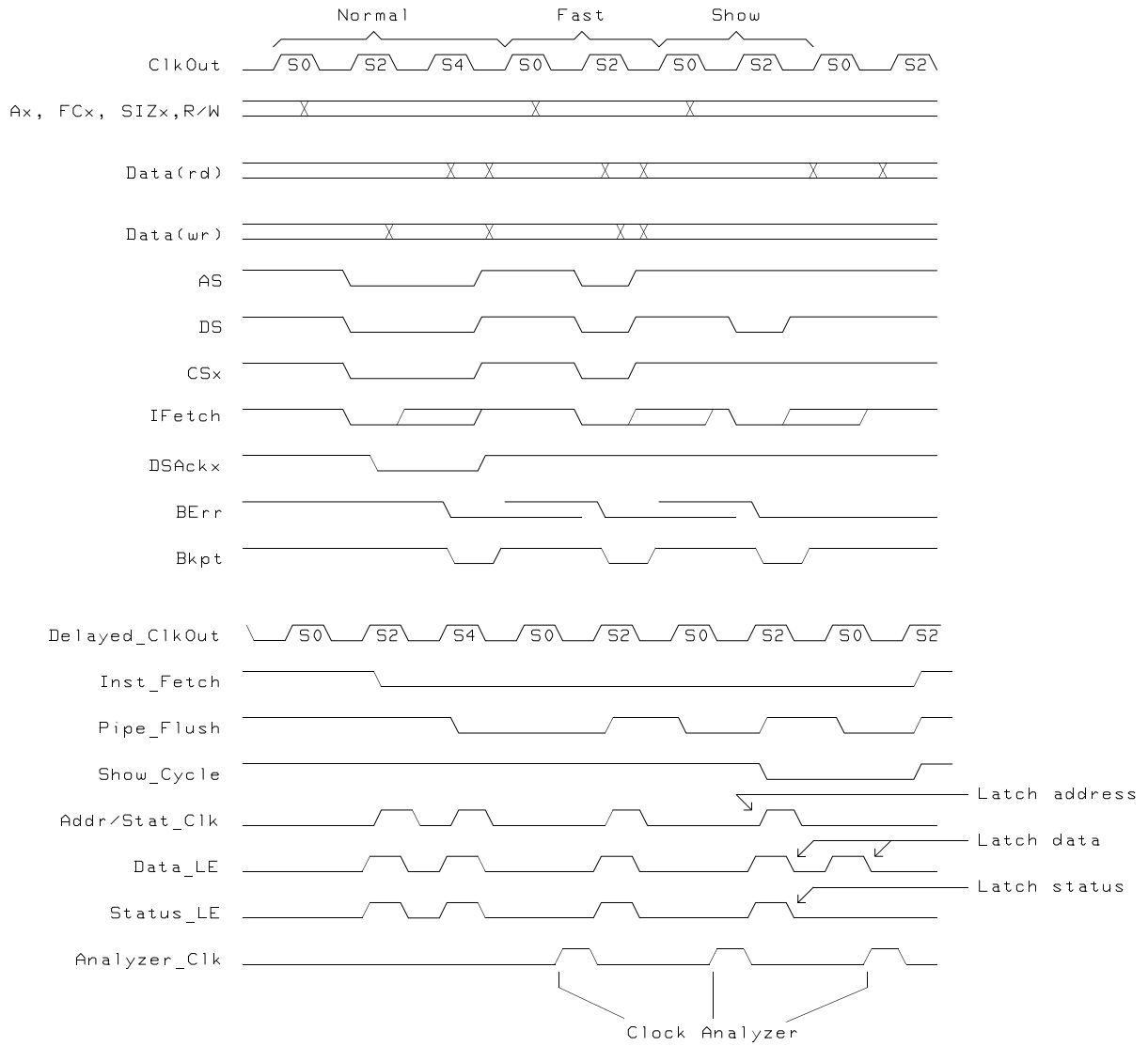
E2439B01

**Block Diagram**

# Preprocessor Interface Hardware Reference

## Theory of Operation and Clocking

The following timing diagram shows the time at which address and data are sampled.



**Timing Diagram**

## Signal-to-Connector Mapping

The following table shows the flow of signals from the MC68332 through the E2413C timing connectors to the logic analyzer. "System Ground" indicates the common ground reference points between the target system and the preprocessor. "Analyzer Bit" indicates the bit definitions.

For analyzers having or using less than 7 pods, "Timing Connector Pin" may be used to perform a user-defined hook-up. In this case, a new configuration will need to be created.

**Table 3-1 MC68332 Signal List**

68332 PIN	68332 SIGNAL NAME	SYSTEM GROUND	E2413C PGA PIN	E2413C TIMING CONNECTOR PIN	ANALYZER BIT	TIMING LABEL
1	VDD		G 8			
2	VSS	X	G 11			
3	TP11		G 12	7- 8	7-11	TPU
4	TP10		G 9	7- 9	7-10	TPU
5	TP9		G 10	7-10	7- 9	TPU
6	TP8		H 11	7-11	7- 8	TPU
7	VDD		H 12			
8	VSS	X	H 9			
9	TP7		H 10	7-12	7- 7	TPU
10	TP6		J 12	7-13	7- 6	TPU
11	TP5		J 10	7-14	7- 5	TPU
12	TP4		J 11	7-15	7- 4	TPU
13	TP3		K 11	7-16	7- 3	TPU
14	TP2		K 12	7-17	7- 2	TPU
15	TP1		L 11	7-18	7- 1	TPU
16	TP0		L 12	7-19	7- 0	TPU
17	VSS	X	M12			
18	VDD		M11			
19	VSTBY		L 10			
20	ADDR1		K 10	2-18	2- 1	ADDR
21	ADDR2		M10	2-17	2- 2	ADDR

Preprocessor Interface Hardware Reference  
**Signal-to-Connector Mapping**

68332 PIN	68332 SIGNAL NAME	SYSTEM GROUND	E2413C PGA PIN	E2413C TIMING CONNECTOR PIN	ANALYZER BIT	TIMING LABEL
22	ADDR3		K 9	2-16	2- 3	ADDR
23	ADDR4		J 9	2-15	2- 4	ADDR
24	ADDR5		M 9	2-14	2- 5	ADDR
25	ADDR6		L 9	2-13	2- 6	ADDR
26	ADDR		K 8	2-12	2- 7	ADDR
27	ADDR8		J 8	2-11	2- 8	ADDR
28	VDD		M 8			
29	VSS	X	L 8			
30	ADDR9		K 7	2-10	2- 9	ADDR
31	ADDR10		J 7	2- 9	2-10	ADDR
32	ADDR11		M 7	2- 8	2-11	ADDR
33	ADDR12		L 7	2- 7	2-12	ADDR
34	VSS		H 6			
35	ADDR13		L 6	2- 6	2-13	ADDR
36	ADDR14		M 6	2- 5	2-14	ADDR
37	ADDR15		J 6	2- 4	2-15	ADDR
38	ADDR16		K 6	3-19	3- 0	ADDR
39	VDD		L 5			
40	VSS	X	M 5			
41	ADDR17		J 5	3-18	3- 1	ADDR
42	ADDR18		K 5	3-17	3- 2	ADDR
43	MISO		M 4	5-18	5- 1	QSM
44	MOSI		K 4	5-19	5- 0	QSM
45	SCK		L 4	5-17	5- 2	QSM
46	PCS0/~SS		L 3	5-13	5- 6	QSM
47	PCS1		M 3	5-14	5- 5	QSM
48	PCS2		L 2	5-15	5- 4	QSM
49	PCS3		M 2	5-16	5- 3	QSM
50	VDD		M 1			
51	VSS	X	L 1			
52	TXD		K 2	5-12	5- 7	QSM
53	RXD		K 3	6- 7	6-12	QSM
54	~IPIPE/DSO		K 1	4-16	4- 3	STAT

68332 PIN	68332 SIGNAL NAME	SYSTEM GROUND	E2413C PGA PIN	E2413C TIMING CONNECTOR PIN	ANALYZER BIT	TIMING LABEL
55	~IFETCH/DSI		J 3	4-17	4- 2	IFETCH
56	~BKPT/DSCLK		J 4	4- 4	4-15	STAT
57	TSC		J 1	6- 5	6-14	TSC
58	FREEZE/QUOT		J 2	4- 5	4-14	STAT
59	VSS		H 3			
60	XTAL		H 4			
61	VDDSYN		H 1			
62	EXTAL		H 2			
63	VDD		G 3			
64	XFC		G 4			
65	VDD		G 1			
66	CLKOUT		G 2	6- 4	6-15	CLKOUT
67	VSS	X	F 5			
68	~RESET		F 2	4-13	4- 6	STAT
69	~HALT		F 1	4-12	4- 7	STAT
70	~BERR		F 4	4- 9	4-10	STAT
71	~IRQ7		F 3	5-11	5- 8	IRQ
72	~IRQ6		E 2	5-10	5- 9	IRQ
73	~IRQ5		E 1	5- 9	5-10	IRQ
74	~IRQ4		E 4	5- 8	5-11	IRQ
75	~IRQ3		E 3	5- 7	5-12	IRQ
76	~IRQ2		D 1	5- 6	5-13	IRQ
77	~IRQ3		D 3	5- 5	5-14	IRQ
78	~IRQ1		D 2	5- 4	5-15	MODCLK
79	R/~W		C 2	4-18	4- 1	R/~W
80	SIZ1		C 1	4-14	4- 5	SIZ10
81	SIZ0		B 2	4-15	4- 4	SIZ10
82	~AS		B 1	4- 6	4-13	AS
83	VSS	X	A 1			
84	VDD		A 2			
85	~DS		B 3	4- 7	4-12	DS
86	~RMC		C 3	4- 8	4-11	STAT
87	~AVEC		A 3	4-19	4- 0	STAT

Preprocessor Interface Hardware Reference  
**Signal-to-Connector Mapping**

68332 PIN	68332 SIGNAL NAME	SYSTEM GROUND	E2413C PGA PIN	E2413C TIMING CONNECTOR PIN	ANALYZER BIT	TIMING LABEL
88	~DSACK1		C 4	4-10	4- 8	~DSAK10
89	~DSACK0		D 4	4-11	4- 9	~DSAK10
90	ADDR0		A 4	2-19	2- 0	ADDR
91	DATA15		B 4	1- 4	1-15	DATA
92	DATA14		C 5	1- 5	1-14	DATA
93	DATA13		D 5	1- 6	1-13	DATA
94	DATA12		A 5	1- 7	1-12	DATA
95	VSS		B 5			
96	VDD		C 6			
97	DATA11		D 6	1- 8	1-11	DATA
98	DATA10		A 6	1- 9	1-10	DATA
99	DATA9		B 6	1-10	1- 9	DATA
100	DATA8		E 7	1-11	1- 8	DATA
101	VSS	X	B 7			
102	DATA7		A 7	1-12	1- 7	DATA
103	DATA6		D 7	1-13	1- 6	DATA
104	DATA5		C 7	1-14	1- 5	DATA
105	DATA4		B 8	1-15	1- 4	DATA
106	VSS	X	A 8			
107	VDD		D 8			DATA
108	DATA3		C 8	1-16	1- 3	DATA
109	DATA2		A 9	1-17	1- 2	DATA
110	DATA1		C 9	1-18	1- 1	DATA
111	DATA0		B 9	1-19	1- 0	DATA
112	~CSBOOT		B 10	3-11	3- 8	CSX
113	~BR/~CS0		A 10	3-10	3- 9	BUSARB
114	~BG/~CS1		B 11	3- 9	3-10	BUSARB
115	~BGACK/~CS2		A 11	3- 8	3-11	BUSARB
116	VDD		A 12			
117	VSS	X	B 12			
118	FC0/~CS3		C 11	3- 7	3-12	FCX
119	FC1		C 10	3- 6	3-13	FCX
120	FC2/~CS5		C 12	3- 5	3-14	FCX



68332 PIN	68332 SIGNAL NAME	SYSTEM GROUND	E2413C PGA PIN	E2413C TIMING CONNECTOR PIN	ANALYZER BIT	TIMING LABEL
121	ADDR19/~CS6		D 10	3-16	3- 3	ADDR
122	ADDR20/~CS7		D 9	3-15	3- 4	ADDR
123	ADDR21/~CS8		D 12	3-14	3- 5	ADDR
124	ADDR22/~CS9		D 11	3-13	3- 6	ADDR
125	ADDR23/~CS10		E 10	3-12	3- 7	ADDR
126	VDD		E 9			
127	VSS	X	E 12			
128	T2CLK		E 11	6- 6	6-13	TPU
129	TP15		F 10	7- 4	7-15	TPU
130	TP14		F 9	7- 5	7-14	TPU
131	TP13		F 12	7- 6	7-13	TPU
132	TP12		F 11	7- 7	7-12	TPU
		shield	E 5			
		shield	E 6			
		shield	E 8			
		shield	F 6			
		shield	F 7			
		shield	F 8			
		shield	G 5			
		shield	G 6			
		shield	G 7			
		shield	H 5			
		shield	H 7			
		shield	H 8			
		X		1-20		
		X		2-20		
		X		3-20		
		X		4-20		
		X		5-20		
		X		6-20		
		X		7-20		

---

## State Connector Signal Definition

The following table defines the state connectors, the logic analyzer bit assignments, and the label/sublabel(s) to which a signal belongs. This table aids in reconfiguring the logic analyzer to match a particular microcontroller configuration.

---

**Table 3-2 E2413C State Connector Signal List**

<b>68332 SIGNAL NAME</b>	<b>E2413C STATE CONNECTOR PIN</b>	<b>ANALYZER BIT</b>	<b>STATE LABEL</b>	<b>STATE SUBLABEL</b>
DATA0	1-37	1- 0	DATA	
DATA1	1-35	1- 1	DATA	
DATA2	1-33	1- 2	DATA	
DATA3	1-31	1- 3	DATA	
DATA4	1-29	1- 4	DATA	
DATA5	1-27	1- 5	DATA	
DATA6	1-25	1- 6	DATA	
DATA7	1-23	1- 7	DATA	
DATA8	1-21	1- 8	DATA	
DATA9	1-19	1- 9	DATA	
DATA10	1-17	1-10	DATA	
DATA11	1-15	1- 1	DATA	
DATA12	1-13	1-12	DATA	
DATA13	1-11	1-13	DATA	
DATA14	1- 9	1-14	DATA	
DATA15	1- 7	1-15	DATA	
ADDR0	2-37	2- 0	ADDR	
ADDR1	2-35	2- 1	ADDR	
ADDR2	2-33	2- 2	ADDR	
ADDR3	2-31	2- 3	ADDR	
ADDR4	2-29	2- 4	ADDR	
ADDR6	2-25	2- 6	ADDR	

---

68332 SIGNAL NAME	E2413C STATE CONNECTOR PIN	ANALYZER BIT	STATE LABEL	STATE SUBLABEL
ADDR7	2-23	2- 7	ADDR	
ADDR8	2-21	2- 8	ADDR	
ADDR9	2-19	2- 9	ADDR	
ADDR10	2-17	2-10	ADDR	
ADDR11	2-15	2-11	ADDR	
ADDR12	2-13	2-12	ADDR	
ADDR13	2-11	2-13	ADDR	
ADDR14	2- 9	2-14	ADDR	
ADDR15	2- 7	2-15	ADDR	
ADDR16	3-37	3- 0	ADDR	
ADDR17	3-35	3- 1	ADDR	
ADDR18	3-33	3-	ADDR	
ADDR19/~CS6	3-31	3- 3	ADDR	CSx
ADDR20/~CS7	3-29	3- 4	ADDR	CSx
ADDR21/~CS8	3-27	3- 5	ADDR	CSx
ADDR22/~CS9	3-25	3- 6	ADDR	CSx
ADDR23/~CS10	3-23	3- 7	ADDR	CSx
<b>NOTE:</b> Signals A19-A23 and CS6-CS10 are multiplexed onto the same pins, and the default configuration of the logic analyzer assumes that signals A19-A23 are valid. If any of the chip selects, CS6-CS10, are being used and the appropriate switch(es) are set to VALID on the preprocessor, then the bits associated with A19-A23 should be removed from the ADDR label via the format menu in the logic analyzer. This corresponds to bits 3-7 of pod A4. This results in the display of correct address information in the ADDR field of the listing menu and presents only valid address bus bits to the ADDR field in the trigger menu.				
~CSBOOT	3-21	3- 8	ADDR_B	CSx
~BR/~CS0	3-19	3- 9	ADDR_B	BusArb CSx
~BG/~CS1	3-17	3-10	ADDR_B	BusArb CSx
~BGACK/~CS2	3-15	3-11	ADDR_B	BusArb CSx
FC0/~CS3	3-13	3-12	ADDR_B	FCx CSx
FC1	3-11	3-13	ADDR_B	FCx CSx
FC2/~CS5	3- 9	3-14	ADDR_B	FCx CSx
UNUSED	3- 7	3-15		

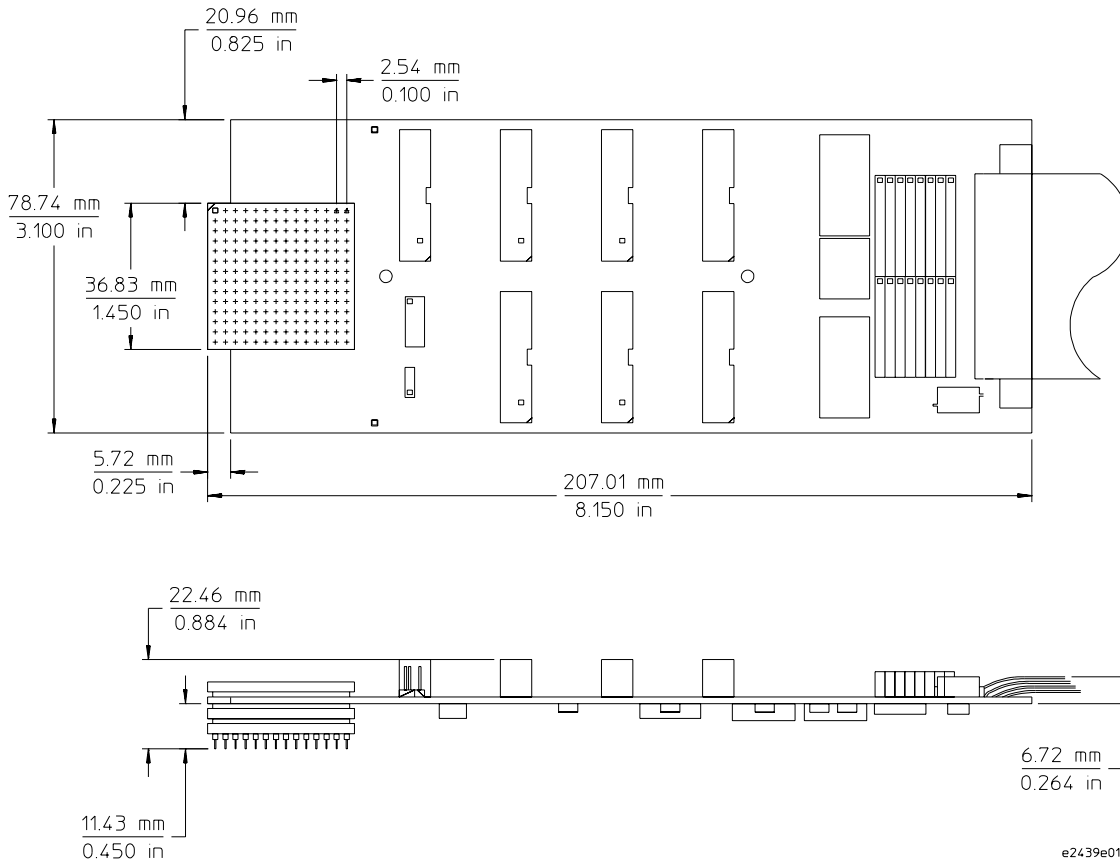
Preprocessor Interface Hardware Reference  
**State Connector Signal Definition**

<b>68332 SIGNAL NAME</b>	<b>E2413C STATE CONNECTOR PIN</b>	<b>ANALYZER BIT</b>	<b>STATE LABEL</b>	<b>STATE SUBLABEL</b>
~SHOW_CYCLE	4-37*	4- 0	STAT	ShoCyc
R/~W	4-35	4- 1	STAT	R/~W
~INST_FETCH	4-33*	4- 2	STAT	IFetch
~PIPE_FLUSH	4-31*	4- 3	STAT	PFlush
SIZ0	4-29	4- 4	STAT	SIZx
SIZ1	4-27	4- 5	STAT	SIZx
~SIZE0_VALID	4-25*	4- 6	STAT	
~SIZE1_VALID	4-23*	4- 7	STAT	
QUALIFIED_DSACK0	4-21*	4- 8	STAT	DSACKx
QUALIFIED_DSACK1	4-19*	4- 9	STAT	DSACKx
~BERR	4-17	4-10	STAT	BErr
~BUS_ARB_INVALID	4-15*	4-11	STAT	
~FCx_INVALID	4-13*	4-12	STAT	
~A19-A23_INVALID	4-11*	4-13	STAT	
FREEZE/QUOT	4- 9	4-14	STAT	Freeze
~BKPT/DSCLK	4- 7	4-15	STAT	Bkpt

Signals having an asterisk (\*) are generated by programmable logic.

## Circuit Board Dimensions

The following figure gives the dimensions for the preprocessor interface assembly. The dimensions are listed in inches and millimeters.



### Dimensions

## Repair Strategy

The repair strategy for this preprocessor interface is board replacement. However, the following table lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Agilent Technologies Sales Office for further information on servicing the board.

Exchange assemblies are available when a repairable assembly is returned to Agilent Technologies. These assemblies have been set up on the "Exchange Assembly" program. This allows you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

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**Table 3-3 Replaceable Parts**

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<b>Part Number</b>	<b>Description</b>
<b>E2413-69506</b>	Circuit board assembly
<b>E2413-68704</b>	Inverse assembler disk pouch
<b>E5081-7736</b>	132-pin PQFP probe adapter assembly
<b>E5359A</b>	144-pin TQFP Elastomeric Probing System Kit (consists of the following parts which can be ordered separately)
<b>E5338A</b>	144-pin TQFP flexible adapter
<b>E5341A</b>	68332 PGA transition socket
<b>E5336A</b>	144-pin TQFP Elastomeric probe adapter
<b>E5336A opt. 201</b>	Retainers (5), knurled nuts (2), and adhesive
<b>E5336A opt. 202</b>	Locator tool

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The Warning symbol calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a Warning symbol until the indicated conditions are fully understood and met.

#### **Caution**

The Caution symbol calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a Caution symbol until the indicated conditions are fully understood or met.

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**About this edition**

This is the *Agilent E2413C  
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Many product updates and fixes do not require manual changes; and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual updates.

All pages original edition